

CLAIMS:

1. Buffer management system (100) for controlling in a data communication system a delay (Δ) of a data unit (150) between input in the buffer management system (100) and output from the buffer management system (100), comprising:
 - a buffer (102), in which blocks (104, 106) of inputted data units (150, 152) are written with a block write rate (R_w), and from which data units (154, 156) are read with a read rate (R_r);
 - a buffer filling measurement component (110) arranged to determine an amount (F) of data units in the buffer (102) at a specified time instant (T_l), and yielding a filling measurement (m_F); and
- 5 10 - a data rate conversion component (108), arranged to set a ratio of the read rate (R_r) and the write rate (R_w), on the basis of the filling measurement (m_F); characterized in that
 - an input time measuring component (112) is comprised, arranged to measure an input time instant (T_a) of input of the data unit (150) in the buffer management system (100), and yielding an input time measurement (m_{Ta}); and
 - a delay control component (120) is comprised for controlling the delay (Δ) by controlling the data rate conversion component (108) on the basis of the filling measurement (m_F) and the input time measurement (m_{Ta}).
- 15 20 2. Buffer management system (100) as claimed in claim 1, comprising a read time measuring component (160), arranged to measure a read time instant (T_r) of a first data unit (154), and yielding a read time measurement (m_{Tr}), and in which buffer management system (100) the delay control component (120) is arranged to control the data rate conversion component (108) on the basis of the read time measurement (m_{Tr}).
- 25 3. Buffer management system (100) as claimed in claim 1 or 2, in which the data rate conversion component (108) comprises a voltage controlled oscillator.

4. **Buffer management system (100) as claimed in claim 1 or 2, in which the data rate conversion component (108) comprises a sample rate converter (514), arranged to produce a second number of samples (142) out of a first number of samples (140).**
5. **5. Buffer management system (100) as claimed in claim 1, comprising a decompressor (512), in which buffer management system the delay control component (120) is arranged to control the data rate conversion component (108) on the basis of a decompression delay associated with the decoder and/or an amount (W) of data units are in a second buffer (506).**
- 10 **6. Digital audio receiver (500) comprising:**
- **a radio reception component (502) with an output (503) connected to**
- **a buffer management system (100) as in claim 1.**
- 15 **7. Headphones (530) comprising a digital audio receiver (500) as claimed in claim 6, an output of the digital audio receiver (500) being connected to a loudspeaker of the headphones.**
8. **Stand-alone surround sound loudspeaker cabinet (540) comprising a digital audio receiver (500) as claimed in claim 6, an output of the digital audio receiver (500) being connected to a loudspeaker (528) in the cabinet.**
- 20 **9. Method of controlling in a data communication system a delay (Δ) of a data unit (150), between input in a digital audio receiver (500) and output from the digital audio receiver (500), comprising:**
- **Writing blocks (104, 106) of inputted data units (150, 152) in a buffer (102) with a block write rate (Rw);**
- **Determining a filling measurement (mF) of an amount (F) of data units in the buffer (102) at a specified time instant (Tl);**
30 **- Setting a ratio of a read rate (Rr) and the write rate (Rw), on the basis of the filling measurement (mF); and**
- **Reading data units (154, 156) from the buffer (102) with the read rate (Rr), the method being characterized in that:**

- an input time measurement (mTa) of an input time instant (Ta) of input of the data unit (150) in the digital audio receiver (500) is performed; and
- the delay (Δ) is controlled by setting the ratio of the read rate (Rr) and the write rate (Rw) also on the basis of the input time measurement (mTa).

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10. Computer program product enabling a processor to execute the method of claim 9.